Model 560-5303
N8 FREQUENCY SYNTHESIZER
(8 kPPS - 8192 kPPS)

Serial Number _____

SECTION ONE

1 FUNCTIONAL DESCRIPTION

1.1 PURPOSE OF EQUIPMENT

The TrueTime 560-5303 N8 Frequency Synthesizer is a plug-in option card for the Model 56000 DRC. In a system that includes a Fault Monitor/CPU card, this option card offers the user six independently programmable frequency synthesizers that provide pulse rates from 8 kPPS through 8192 kPPS in 8 kPPS steps. In CPU controlled applications, the 560-5303 card uses nine DIP switches to provide any one of the 1024 different frequency rates to all six outputs.

The N8 Frequency Synthesizer generates an output frequency that is locked to the external reference frequency distributed via REF A, B, or C from the backplane. The input frequency from the REF A, B, and C inputs is switch-selectable as a group (1, 5, or 10 MHz) by an on-card DIP switch. The reference is received via the Fast Switch Circuit, which passes only the currently-highest priority reference to the synthesizer. If the currently-highest priority reference is changed, the Fast Switch Circuit shifts to the next-highest priority input and the synthesizer locks to the new reference.

In a system without a Fault Monitor CPU card, the N8 Frequency Synthesizer card offers automatic REF A, B, C Fast Switch Circuit operation up to 4096 MHz, as previously stated. When the N8 card is used in a system that includes the Fault Monitor CPU card, the REF A, B, C inputs are also controlled by the CPU. When a REF A source's Fault Status is detected (monitored by the CPU), the REF A input on the N8 card is disabled. The REF B and REF C inputs are operated similarly – they are turned off whenever a Fault Status condition for that reference exists. The CPU's REF A, B, C control feature ensures that only a viable reference oscillator is used on the 560-5303 N8 card. For a reference signal that later becomes viable, requires operator intervention.

The N8 Frequency Synthesizer also has the capability of synchronizing the phase of the frequency outputs. The six on-board synthesizers may be synchronized (reset) with a signal from the Model 56000 backplane timing inputs (INPUT 1 through INPUT 8). This synchronization allows the N8 frequency rates to not only be frequency locked but to also be phase coherent to all of the other outputs on the card(s). NOTE: When the N8 Frequency Synthesizer is used in a system with a Fault Monitor/CPU card, only the synthesizer IC that is given a new frequency value will be re-synchronized. In a system without a CPU card, all six synthesizer ICs are synchronized once at turn-on.

The N8 frequency that is generated is output through the backplane connector via six complementary drivers. The output signals are delivered to external cables via the I/O card installed in the rear slot directly behind the N8 synthesizer. Output drive capability is switch-selectable for RS-422 / 100 ohm or TTL / 50 ohm. NOTE: The TTL setting provides

enhanced drive capability, and allows the short circuit current to exceed the RS-422 specification. The output mode, single-ended or differential, is determined by the type of I/O card that is installed.

1.2 PHYSICAL SPECIFICATIONS

Dimensions:	0.8”w X 3.94”h X 8.66”d (2 cm X 10 cm X 22 cm)
Weight:	Approximately ½ pound (¼ kg)

1.3 ENVIRONMENTAL SPECIFICATIONS

Operating Temp:	0° to +50°C
Storage Temp:	-40° to +85°C
Humidity:	Up to 95% relative, non-condensing
Cooling Mode:	Convection
Altitude	Sea Level to 10,000 ft.

1.4 POWER REQUIREMENTS

Voltage:	18-72 VDC
Power:	7 W (outputs A through F driving 50 Ω)

1.5 FUNCTIONAL SPECIFICATIONS

1.5.1 REF A, B, and C INPUTS

Signal Type:	Squarewave or Sinewave
Amplitude:	2-5 Vp-p
Frequency:	1, 5, or 10 MHz (switch-selectable)

1.5.2 TTL OUTPUTS (SW3-4 = ON)

Quantity:	6
Signal Type:	Squarewave, TTL-level
Amplitude:	2.8 Vpk into 50 ohms

1.5.3 RS-422 OUTPUTS (SW3-4 = OFF)

Quantity:	6
Signal Type:	Squarewave, centered at 2.5 VDC
Amplitude:	2.8 Vp-p into 100 ohms
Output Drive	MIL-STD-188-114A TYPE II
Compliance:	BALANCED RS-422-A

1.5.4 OUTPUT FREQUENCY

Frequencies:	8 kPPS to 8192 kPPS in 8 kPPS steps
Frequency Stability:	
Long-term:	Equal to reference on REF A, B, or C
Short-term:	Better than 1 part in 10^9 (1 second average)
Timing:	Rising Edge < 500 ns output to output (for rates 64 kPPS and above)
Phase noise:	-50 dBc/√Hz @ 4 Hz from carrier
Spurious:	-60 dBc

1.5.5 CARD COMPATIBILITY

Location:	Slot 1-17 with compatible I/O card in rear slot.
Compatibility:	See Card Compatibility Matrix.

SECTION TWO

2 INSTALLATION AND OPERATION

2.1 HOT SWAPPING

All cards, input cables, and output cables are hot swappable. It is not necessary to remove chassis power during insertion or removal. Hot swapping and reference-source changes are abrupt, the effects difficult to characterize; however, the system is designed to protect against permanent effects and minimize temporary effects of these events. Typically, adjacent-card hot swapping has a negligible effect on the N8 Frequency Synthesizer. Although the hot swapping event directly affects the control voltage of each on-board oscillator, it typically lasts less than one clock-period and has an average of 0 Volts. The effect of redundant power supply switch-over is also negligible.

The effect of a reference-source change is less predictable. The reference frequency is delivered via REF A, B, and C on the backplane. The N8 Frequency Synthesizer receives the reference via the Passive Combiner. If the currently-highest priority reference is changed, the Synthesizer locks to the new reference. When the new reference is in phase with the old reference, the output frequency is affected by less than 1 part in 10^8 over a 1 second period. When the new reference is of opposite phase, the effect can approach 1 part in 10^6. The frequency shift occurs relatively softly over a 100 ms period, minimizing any effect on downstream equipment. Note that hot swapping a local frequency source, such as an oscillator or fiber optic receiver, qualifies as a hot swap and reference-source change.

The effect of a reference-input perturbation that does not result in a reference-source change (e.g. - removing a cable that is not currently highest priority) at the passive combiner also has an effect on the N8 Frequency Synthesizer. This is due to the fact that the reference frequency used by the synthesizer is always a weighted sum of REF A, B, and C, and any change has some effect on the resultant waveform. The effect is usually negligible, but can approach 1 part in 10^8.

2.2 REMOVAL AND INSTALLATION

CAUTION: Individual components on this card are sensitive to static discharge. Use proper static discharge procedures during removal and installation.

Refer to CARD COMPATIBILITY section prior to installing new card.

To remove card, loosen the captive retaining hardware at the top and bottom of the assembly, then firmly pull on the handle (or on any connector on rear panel adapter cards) at the bottom of the card. Slide the card free of the frame. Refer to the SETUP section for any required switch settings; or, set them identically to the card being replaced.

Reinstall the card in the frame by fitting it into the card guides at the top and bottom of the frame and sliding it in slowly, avoiding contact between bottom side of card and adjacent card front panel, until it mates with the connector. Seat card firmly to avoid contact bounce. Secure the retaining screws at the top and bottom of the card assembly.

2.3 SETUP

The setup of the 560-5303 N8 Frequency Synthesizer card involves setting the following DIP switches:

Required switch settings:

1. Input Frequency Select Switch (SW3-2 & SW3-3)
2. Output Drive Select Switch (SW3-4)
3. CPU / LOCAL Mode Select (SW7-4)
4. Output Frequency Selection Switches (SW4-3 & SW3-1)
   (used only in local mode)

To align the rising edge of the outputs (phase synchronize) with other N8 outputs in the system, the following switches must be set:

6. Primary Synch Input Switch (SW1)
7. Secondary Synch Input Switch (SW2)
8. Primary Synch Input Enable Switch (SW5)
9. Secondary Synch Input Enable Switch (SW6)
10. Delay Switch (activity time-out) (SW7-1 through SW7-3)

2.3.1 INPUT FREQUENCY SELECT SWITCH (SW3-2 & SW3-3)

This switch sets the internal divider for the PLL control. This switch MUST be set to match the input frequency in use on REF A, B, and C.

INPUT FREQUENCY SELECT	SW3-2	SW3-3
1 MHz	OFF	OFF
5 MHz	OFF	ON
10 MHz	ON	OFF

2.3.2 OUTPUT DRIVE SELECT SWITCH (SW3-4)

Set SW3-4 to select the output drive mode:

SW3-4	ON: TTL / 50 ohms
SW3-4	OFF: RS-422 / 100 ohms

2.3.3 CPU / LOCAL MODE SELECT SWITCH (SW7-4)

SW1-4 is the CPU / LOCAL select switch. If the switch is ON, the card will be operated in LOCAL mode, which uses the nine on-board frequency setting switches to select one frequency rate for all six outputs. If the switch is OFF, the card will be operated in CPU mode, which allows independent serial port control on each of the six outputs.

SW7-4 CPU Mode	OFF
SW7-4 LOCAL Mode	ON

2.3.4 LOCAL MODE FREQUENCY SELECTION SWITCHES (SW4 & SW3-1)

These nine switches set 1 of the 1024 possible frequency rates that all six synthesizers will generate. These switches MUST be set for the desired frequency rate when the N8 card is operated in LOCAL mode (not programmable via CPU card).

Note: For enhanced mode operation (frequencies above 4096 kPPS), select the frequencies using CPU Mode (Section 2.4). For CPU mode, set SW7-4 to OFF.

SW3 has eight switch bits which are named 1 through 8 in the following frequency setting table. SW7-1 is the LSB and is named switch 1 in the table. SW3-1 is the MSB and is named switch 9 in the table.

(Frequency x 1 kPPS)

Switches	**OFF**	**6**	**7**	**7+6**	**8**	**8+6**	**8+7**	**8+7+6**	**9**	**9+6**	**9+7**	**9+7+6**	**9+8**	**9+8+6**	**9+8+7**	**9+8+7+6**
OFF	4096	256	512	768	1024	1280	1536	1792	2048	2304	2560	2816	3072	3328	3584	3840
1	8	264	520	776	1032	1288	1544	1800	2056	2312	2568	2824	3080	3336	3592	3848
2	16	272	528	784	1040	1296	1552	1808	2064	2320	2576	2832	3088	3344	3600	3856
2+1	24	280	536	792	1048	1304	1560	1816	2072	2328	2584	2840	3096	3352	3608	3864
3	32	288	544	800	1056	1312	1568	1824	2080	2336	2592	2848	3104	3360	3616	3872
3+1	40	296	552	808	1064	1320	1576	1832	2088	2344	2600	2856	3112	3368	3624	3880
3+2	48	304	560	816	1072	1328	1584	1840	2096	2352	2608	2864	3120	3376	3632	3888
3+2+1	56	312	568	824	1080	1336	1592	1848	2104	2360	2616	2872	3128	3384	3640	3896
4	64	320	576	832	1088	1344	1600	1856	2112	2368	2624	2880	3136	3392	3648	3904
4+1	72	328	584	840	1096	1352	1608	1864	2120	2376	2632	2888	3144	3400	3656	3912
4+2	80	336	592	848	1104	1360	1616	1872	2128	2384	2640	2896	3152	3408	3664	3920
4+2+1	88	344	600	856	1112	1368	1624	1880	2136	2392	2648	2904	3160	3416	3672	3928
4+3	96	352	608	864	1120	1376	1632	1888	2144	2400	2656	2912	3168	3424	3680	3936
4+3+1	104	360	616	872	1128	1384	1640	1896	2152	2408	2664	2920	3176	3432	3688	3944
4+3+2	112	368	624	880	1136	1392	1648	1904	2160	2416	2672	2928	3184	3440	3696	3952
4+3+2+1	120	376	632	888	1144	1400	1656	1912	2168	2424	2680	2936	3192	3448	3704	3960
5	128	384	640	896	1152	1408	1664	1920	2176	2432	2688	2944	3200	3456	3712	3968
5+1	136	392	648	904	1160	1416	1672	1928	2184	2440	2696	2952	3208	3464	3720	3976
5+2	144	400	656	912	1168	1424	1680	1936	2192	2448	2704	2960	3216	3472	3728	3984
5+2+1	152	408	664	920	1176	1432	1688	1944	2200	2456	2712	2968	3224	3480	3736	3992
5+3	160	416	672	928	1184	1440	1696	1952	2208	2464	2720	2976	3232	3488	3744	4000
5+3+1	168	424	680	936	1192	1448	1704	1960	2216	2472	2728	2984	3240	3496	3752	4008
5+3+2	176	432	688	944	1200	1456	1712	1968	2224	2480	2736	2992	3248	3504	3760	4016
5+3+2+1	184	440	696	952	1208	1464	1720	1976	2232	2488	2744	3000	3256	3512	3768	4024
5+4	192	448	704	960	1216	1472	1728	1984	2240	2496	2752	3008	3264	3520	3776	4032
5+4+1	200	456	712	968	1224	1480	1736	1992	2248	2504	2760	3016	3272	3528	3784	4040
5+4+2	208	464	720	976	1232	1488	1744	2000	2256	2512	2768	3024	3280	3536	3792	4048
5+4+2+1	216	472	728	984	1240	1496	1752	2008	2264	2520	2776	3032	3288	3544	3800	4056
5+4+3	224	480	736	992	1248	1504	1760	2016	2272	2528	2784	3040	3296	3552	3808	4064
5+4+3+1	232	488	744	1000	1256	1512	1768	2024	2280	2536	2792	3048	3304	3560	3816	4072
5+4+3+2	240	496	752	1008	1264	1520	1776	2032	2288	2544	2800	3056	3312	3568	3824	4080
5+4+3+2+1	248	504	760	1016	1272	1528	1784	2040	2296	2552	2808	3064	3320	3576	3832	4088

2.3.5 PRIMARY SYNCHRONIZATION INPUT SWITCH (SW1)

Set <u>one</u> of the eight SW1 switches to the ON position. The SW1 switch number (1 through 8) corresponds to the INPUT 1 through INPUT 8 signals that are distributed on the backplane. The Primary Synch Input is used to phase synchronize the synthesizer outputs.

PRIMARY SYNC INPUT SW12	**-1**	**-2**	**-3**	**-4**	**-5**	**-6**	**-7**	**-8**
INPUT 1	**ON**	OFF	OFF	OFF	OFF	OFF	OFF	OFF
INPUT 2	OFF	**ON**	OFF	OFF	OFF	OFF	OFF	OFF
INPUT 3	OFF	OFF	**ON**	OFF	OFF	OFF	OFF	OFF
INPUT 4	OFF	OFF	OFF	**ON**	OFF	OFF	OFF	OFF
INPUT 5	OFF	OFF	OFF	OFF	**ON**	OFF	OFF	OFF
INPUT 6	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	OFF
INPUT 7	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	OFF
INPUT 8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	**ON**

2.3.6 SECONDARY SYNCHRONIZATION INPUT SWITCH (SW2)

Set one of the eight SW2 switches to the ON position. The SW2 switch number (1 through 8) corresponds to the INPUT 1 through INPUT 8 signals that are distributed on the backplane. The Secondary Synch Input is used to phase synchronize the synthesizer outputs.

SECONDARY SYNC INPUT SW2	-1	-2	-3	-4	-5	-6	-7	-8
INPUT 1	**ON**	OFF	OFF	OFF	OFF	OFF	OFF	OFF
INPUT 2	OFF	**ON**	OFF	OFF	OFF	OFF	OFF	OFF
INPUT 3	OFF	OFF	**ON**	OFF	OFF	OFF	OFF	OFF
INPUT 4	OFF	OFF	OFF	**ON**	OFF	OFF	OFF	OFF
INPUT 5	OFF	OFF	OFF	OFF	**ON**	OFF	OFF	OFF
INPUT 6	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	OFF
INPUT 7	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	OFF
INPUT 8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	**ON**

2.3.7 PRIMARY SYNCHRONIZATION ENABLE SWITCH (SW5)

This switch should be set to a binary representation of the SW1 setting, the Primary Synchronization Input switch. This switch is also read by the Fault Monitor CPU card which can provide status information to the user.

PRIMARY SYNC ENABLE	SW5-1	SW5-2	SW5-3	SW5-4
INHIBIT	OFF	OFF	OFF	OFF
INPUT 1	ON	OFF	OFF	OFF
INPUT 2	OFF	ON	OFF	OFF
INPUT 3	ON	ON	OFF	OFF
INPUT 4	OFF	OFF	ON	OFF
INPUT 5	ON	OFF	ON	OFF
INPUT 6	OFF	ON	ON	OFF
INPUT 7	ON	ON	ON	OFF
INPUT 8	OFF	OFF	OFF	ON

This switch is also used to disable the Primary synchronization input. If SW5 switches 1 through 4 are OFF, the card will inhibit operation and fault reporting of the Primary synchronization input.

2.3.8 SECONDARY SYNCRONIZATION ENABLE SWITCH (SW6)

This switch should be set to a binary representation of the SW2 setting, the Secondary Synchronization Input switch. This switch is also read by the Fault Monitor CPU card which can provide status information to the user.

SECONDARY SYNC INPUT ENABLE	SW6-1	SW6-2	SW6-3	SW6-4
INHIBIT	OFF	OFF	OFF	OFF
INPUT 1	ON	OFF	OFF	OFF
INPUT 2	OFF	ON	OFF	OFF
INPUT 3	ON	ON	OFF	OFF
INPUT 4	OFF	OFF	ON	OFF
INPUT 5	ON	OFF	ON	OFF
INPUT 6	OFF	ON	ON	OFF
INPUT 7	ON	ON	ON	OFF
INPUT 8	OFF	OFF	OFF	ON

This switch is also used to disable the Secondary synchronization input. If SW6 switches 1 through 4 are OFF, the card will inhibit operation and fault reporting of the Secondary synchronization input.

2.3.9 DELAY SWITCH (SW7 Switches 1, 2, & 3)

SW1 switches 1 through 3 are used to set the time-out delay for input synchronization activity detection. The user should set the delay for a time-out value that is the closest to but longer than the period of the input signal.

Example Setting: If the synchronization input signal is 1 PPS (1 second period), the appropriate setting would be: SW7-1 OFF, SW7-2 OFF, SW7-3 ON – (2.5 second time-out).

DELAY (TIME-OUT)	SW7-1	SW7-2	SW7-3
250 microseconds	OFF	OFF	OFF
2.5 milliseconds	ON	OFF	OFF
25 milliseconds	OFF	ON	OFF
250 milliseconds	ON	ON	OFF
2.5 seconds	OFF	OFF	ON
25 seconds	ON	OFF	ON
125 seconds	OFF	ON	ON
INFINITE	ON	ON	ON

If infinite delay has been selected, fault detection of the Primary and Secondary synchronization inputs is disabled.

2.4 CPU MODE FREQUENCY SELECTION

When the N8 card is set for CPU mode, SW7-4 OFF, the on-card SW4 and SW3 frequency setting switches are not used to set the N8 output frequency rate. The CPU mode allows the six N8 outputs to be set independently via the serial port on the Fault Monitor/CPU card. Use the following serial port syntax to control the frequency rate on OUT A through F.

Use the following ASCII string (upper or lower-case characters) to set the desired frequency rate for output A through F:

Cn<SP>x<SP>f<CR>

where:

C	=	ASCII character “C”
n	=	Card (slot) number (ASCII character(s) “1” through “17”)
<SP>	=	Space character (hex 20)
x	=	Output A, B, C, D, E, or F (ASCII characters)
f	=	Frequency rate (ASCII character(s) “8” through “8192”) (refer to the previous table for valid N8 frequency rates)
<CR>	=	Carriage return (hex OD)

Example entry:

C4 A 2048 (Card Slot #4, Output A, set for 2048 kPPS)

Example response:

C4 A 2048 kPPS

To request the settings for all four outputs on Card Slot #4, send the following ASCII string:

C4? and the serial port will respond with (example):

4, 5303 N8 Frequency Synthesizer
C4 A 0008
C4 B 2048
C4 C 4096
C4 D 1544
C4 E 0008
C4 F 2048

The serial port does not respond to input value errors – the value entry is automatically adjusted to the next viable N8 rate.

The serial port responds to input syntax errors with the following ASCII string:

ERROR 02 SYNTAX<CR><LF>

2.5 FAULT INDICATIONS

All indicators activate briefly following hot-insertion or power-up. The following paragraphs describe operation during steady-state conditions.

2.5.1 SYNTH. FAULT

The Synthesizer Fault indicator may flash briefly during hot swapping and at the addition or removal of REF A, B, or C. This is a normal condition that occurs as the Voltage Controlled Oscillator (VCO) experiences a reference perturbation (see HOT SWAPPING section for a discussion of the effects of hot swapping).

A continuously flashing indication shows either a phase-locked loop out-of-lock condition or, when enabled, the loss of both Primary and Secondary input synchronization inputs. A solid ON SYNTH FAULT LED indicates a local power supply failure.

Loss-of-lock (blinking SYNTH FAULT LED) could be caused by:

1 Input reference off-frequency.

2) Loss of reference on REF A, B, and C. When all references are lost, the VCO drifts to one end of the control range, which is detected as a SYNTH FAULT.

3) A VCO Failure.

2.5.2 OUT. FAULT

The OUT A through OUT F Fault indicators activate when the associated driver has failed. When the card is in the RS-422 output mode, a failure of either the +Output or -Output will activate the indicator, whether or not both outputs are available at the rear I/O Card connector. When the card is in the TTL output mode, only the OUT A through F outputs are fault detected. Note that the detector is designed to detect failed drivers and, typically, will not detect a shorted output.

2.5.3 INIT. FAULT

This is an on-card fault indicator that is not externally visible; although it can be seen by installing the card next to an empty slot. It indicates a failure of the card to initialize properly during power-up. Activation of this LED is accompanied by activation of all of the front panel indicators. Occasionally, this fault is caused by a temporary condition related to the cycling of power and can be cleared by a power or hot swap cycle. If this is unsuccessful, the card is defective.

2.5.4 DETAILED FAULT STATUS VIA CPU

The Fault Monitor CPU has access to detailed 560-5303 card status. This status is available via the Fault Monitor CPU serial port. When it is presented in a 2-byte format, with individual bit definitions as follows:

The Verbose report displays the Fault status. In this context, a reported fault indicates a problem. The Machine report, when used, reports the current status (settings) of the switches and faults in hexadecimal characters. Together, they pinpoint problems and help the technician view the switch settings on the cards without removing them.

2.5.5 VERBOSE REPORTS

The following is an example of a Fault Monitor CPU report in Verbose mode:

TrueTime 56000 Site 01
Automatic Reports **Enabled**
Periodic Reports **Disabled**
Primary Inputs Selected REFA No REFB No REFC Off PRI OK SEC OK TER Off

1. Undefined	OK	Undefined	OK
2. Undefined	OK	Undefined	OK
3. 5303-1	**A-8 DIG FRQ CU**	**FAULT 0407**	**OK**
4. Undefined	OK	Undefined	OK

The above sample tells you that:
Automatic reports are enabled and Periodic reports are disabled. Primary inputs REF A and REF B are not bussing AUX REF. REF C is off. Primary and Secondary inputs OK, Tertiary is OFF.

Numbers 1-4 are slots (not all slots are shown in the example). Slots 1,2,and 4 are undefined (empty) and functional (OK).

Slot 3 is read as follows:
5303 is the abbreviation of the 560-5303 card. The fault reading is 0407.

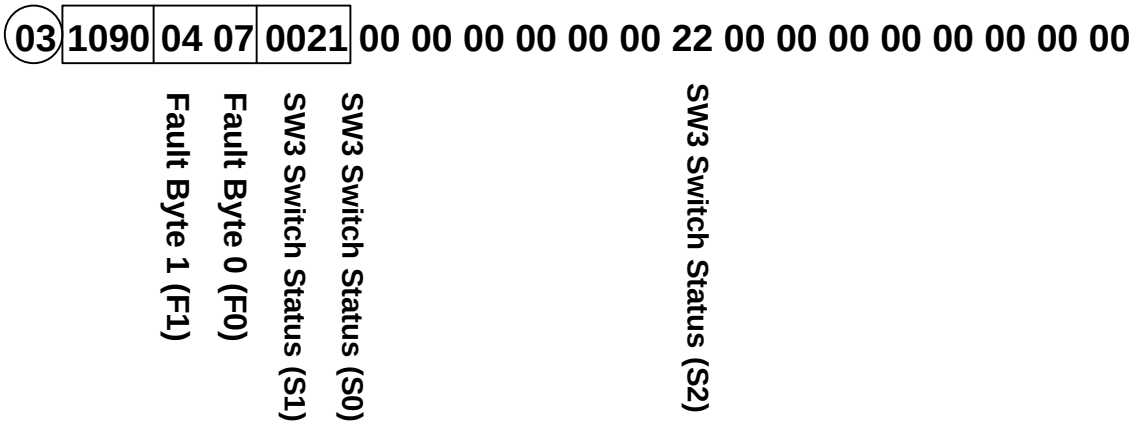
2.5.6 MACHINE REPORTS

The Fault Monitor CPU has another serial output mode called machine report mode. This mode is usually used with a computer program to interrogate the 56000 system status.
The machine report mode displays hexadecimal (HEX) characters like the verbose mode report.

The following is an example of a Fault Monitor CPU report in Machine Mode:

TrueTime 56000 Site 01
AR1
PR10
P A1 B1 Co P1 S1 To
01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
03 10 90 04 07 0021 00 00 00 00 00 00 **02** 00 00 00 00 00 00 00 00 00
04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
(card slots 05 through 14 HEX not shown)

Example from card slot 3 above:



Slot 3 shows that the Fault status is 0407 (F1, F0). The Status report read-out is 0207(S1, S0) and S2 for S2 Status report.

2.5.7 REPORT CONVERSIONS

This section deals with how to read and convert the Fault and Status read-outs using various tables and binary conversions. To decipher a Fault Status report, use Fig. A.
For Status reports (S2, S1, S0) use Fig. B.

FIG. A

Spare	Spare	Spare	Spare	Primary Source	Sec. Input Inactive*	Pri. Input Inactive*	Power Cycled	Undefined	Synthesizer*	Output Fault E*	Output Fault D*	Output Fault C*	Output Fault B*	Output Fault A*	Output Fault F*
8	**4**	**2**	**1**	**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**
2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
0	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*1*	*1*
Upper Byte High Nibble			**0**	Upper Byte Low Nibble			**4**	Lower Byte High Nibble			**0**	Lower Byte Low Nibble			**7**

Fault Status F1 Report Fault Status F0 Report

Key:

Above each 8,4,2,1 is the corresponding fault for that bit. For instance, above the 8 bit in the Upper byte/Low nibble reads Rub. Lockmon, which is the fault .

Shaded area
Informational only. The upper row: Bit value hex weights (8,4,2,1) The Lower row corresponds to the hex weight above. For instance, 2^3 is 8 in binary.
Each section of 8,4,2,1 is a nibble of either an Upper or Lower byte and separated for easy recognition. Each nibble = 4 bits and each byte = 8 bits. "04" is the F1 report, "07" the F0 report.

Non-shaded area
This area is used according with the report read-out after a report is converted to binary. The 0407 is an example from a report.

Always read the report from Upper (High) byte to Lower (Low) Byte.

****** Bit set when bit errors are detected in IRIG-B.

******* These controls are not implemented at this time.
***** Latched Fault Bit – Reset Via Fault Monitor CPU.

Always read the report from Upper (High) byte to Lower (Low) Byte.

Status (S2, S1, S0) Conversion Table **FIG. B**

STATUS REG 0	Bit	Bit Value	Switch	
Low	0	1	Pri Sync Enable SW5-1	
Nibble	1	2	Pri Sync Enable SW5-2	**1**
Low	2	4	Pri Sync Enable SW5-3	
Byte	3	8	Pri Sync Enable SW5-4	
High	4	1	Sec Input Enable SW6-1	
Nibble	5	2	Sec Input Enable SW6-2	**2**
Low	6	4	Sec Input Enable SW6-3	
Byte	7	8	Sec Input Enable SW6-4	
STATUS REG 1				
Low	0	1	Freq Set Switch SW4-1	
Nibble	1	2	Freq Set Switch SW4-2	**0**
High	2	4	Freq Set Switch SW4-3	
Byte	3	8	Freq Set Switch SW4-4	
High	4	1	Freq Set Switch SW4-5	
Nibble	5	2	Freq Set Switch SW4-6	
High	6	4	Freq Set Switch SW4-7	**0**
Byte	7	8	Freq Set Switch SW4-8	
STATUS REG 2				
Low	0	1	Freq Set Switch SW3-1	
Nibble	1	2	Input Freq Select Switch SW3-2	**2**
Low	2	4	Input Freq Select Switch SW3-3	
Byte	3	8	TTL Mode SW3-4	
High	4	1	Delay timeout SW7-1	
Nibble	5	2	Delay timeout SW7-2	**2**
High	6	4	Delay timeout SW7-3	
Byte	7	8	Always 0 (In CPU mode)	

Notes: The settings listed under the Switch column are HIGH or ON. For instance, frequency has SW 7-1 and SW 7-2. If SW 7-1 is ON, SW 7-2 is presumed to be OFF (although there is no specific mention of this). For switches, a 1 = ON, 0 = OFF.
* Latched Fault Bit—Reset Via Fault Monitor CPU

BINARY CONVERSION TABLE

Decimal	Displayed in report as	Binary
0	0	0
1	1	1
2	2	10
3	3	11
4	4	100
5	5	101
6	6	110
7	7	111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Binary:
1 = Fault/Switch On
0 = No Fault/Switch Off

Use the Binary Conversion table to convert a read-out from the monitor to binary. For instance, if the report read-out was 3C15, this would be:

11\1100\1\101 in binary.

USING THE FAULT STATUS REPORT (F0,F1)

The hex weight (fault importance) has been assigned 8, 4, 2, 1. Beneath each number is the corresponding fault. Use Fig. A. The report example read 0407. The 0 is high byte/high nibble, the 4, high byte/low nibble, the 0, low byte/high nibble and 7, low byte/low nibble. Each nibble falls under a section on Fig. A, high to low or left to right.

Look at Fig. A. Below this is a sample read-out. This read-out would appear on the monitor when a Verbose report is requested. In the example, there are no faults in the upper byte/high nibble or in the lower byte/high nibble because both are zero (0). In the upper byte/low nibble, a 4 is reported. Looking directly above this, a 4 bit is easily spotted. The fault is Secondary Input Inactive. However, In the lower byte/low nibble a 7 is reported. There is no 7 listed, only a 1, 2, 4, 8. Use the Binary Conversion table to determine the faults.

Seven (7) is converted to 111 in Binary. In Binary, a 1 = fault and 0 = no fault. Read 111 from right (low bit) to left (high bit) using the lower byte/low nibble group. The first three (from low bit to high bit) are 1's, indicating there is a fault with the Output Faults A, B and F.

Note that the hex weight assigned totals to 7 (4+2+1). If the 7 had been a 6, in binary this is 110. Reading from low bit to high bit, the 1's (i.e.,

faults) fall under hex weight 4 and 2, which equals a hex weight of 6. Of course, glancing at the lower byte/low nibble, you can quickly see (without converting to binary) that under 4 and 2 (i.e., 6) are the Output B and Output A that are in fault.

Each of the four nibbles is grouped by category for easy visual identification of an offending fault. Each nibble has 15 possible fault combinations. All faults are asserted as a logic 1. The faults are latched on the Oscillator card and must be cleared by the 560-5303 Fault Monitor CPU “CL” command.

USING THE STATUS REPORT (S2, S1, S0)

The method used for reading the Fault report is the same when reading the Status report. Refer to Fig. B.

Using the read-out, 0021, but because the table is different, the 0 is located at the high byte(8) of S1. The rest of the numbers follow upward towards the low byte and ending in Status 0. In this case, the 2 falls in the low byte section of Status 0(high nibble\low byte). Indicating that the Sec Input Enable SW6-2. The 1 falls in the low nibble\low byte section of Status 0. This indicates the Pri Sync Enable SW5-1 is active.

1 = Active, 0 = Not active.

In the Status Reg 2 area, there are two 2's. These indicate the following are active:

Input Freq Select Switch SW3-2
Delay timeout SW5-2

SW2-2 Sets for 10 MHz
SW2-4 Sets for TTL output
SW1-2 Sets delay to 25 ms
SW1-4 Sets for CPU mode

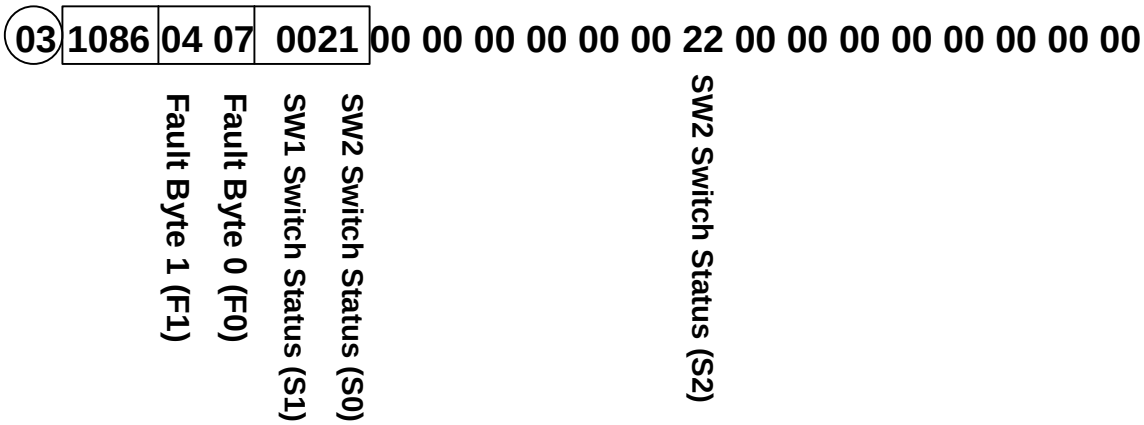
QUICK REFERENCE SHEET FOR READING FAULT AND STATUS REPORTS

1. Run a report. This is a portion of a sample Machine report.

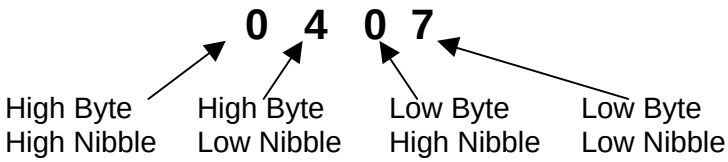
TrueTime 56000 Site 01
AR1
PR10
P A1 B1 Co P1 S1 To
01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
03 10 86 04 07 00 21 00 00 00 00 00 00 **22** 00 00 00 00 00 00 00 00
04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
(card slots 05 through 14 HEX not shown)

0407 is the Fault Status read-out
0021 is the Status read-out report

04 = Fault Status 1 (F1) report
07 = Fault Status 0 (F0) report
00 = Status 1 (S1) report
21 = Status 0 (S0) report



What's in a number?



2. When required, convert Decimal to Binary using the Binary Conversion Table.

BINARY CONVERSION TABLE

Decimal	Displayed in report as	Binary
0	0	0
1	1	1
2	2	10
3	3	11
4	4	100
5	5	101
6	6	110
7	7	111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Binary:
1 = Fault/On/Active
0 = No Fault/Off/Not Active

SECTION THREE

3 THEORY OF OPERATION

3.1 GENERAL INFORMATION

This section contains a detailed description of the circuits used on the N8 Frequency Synthesizer card. Use these descriptions in conjunction with the drawings in SECTION FOUR.

3.2 HARDWARE DESCRIPTION

The N8 Frequency Synthesizer incorporates a passive combiner, a DC-to-DC Converter, a phase-locked VCO, six DDS (Direct Digital Synthesis) ICs to generate the six output frequency rates, 12 Output Drivers (six differential pairs), Fault-detection circuitry and 7 Fault Indicators.

3.3 DETAILED DESCRIPTION

Reference drawing 560-5303.

3.3.1 POWER SUPPLY (Sheet 10)

The DC-to-DC Converter converts 48 VDC backplane power to local ±5 VDC power. It is fully-isolated from the backplane power and referenced to signal GND on the N8 Synthesizer card. Backplane power is supplied via a Polyswitch fuse device, diode and Pi-section L-C filter. The poly-fuse protects the backplane power bus from internal DC-to-DC shorts. The diode and L-C filter serve a triple purpose. During live insertion, the high-current inductor minimizes in-rush current to the DC-to-DC being inserted; and, the diode and capacitor serve to hold up the local voltage at the input to each currently-installed DC-to-DC. During steady-state conditions, the L-C filter minimizes switching noise coupled back into the backplane power bus. During live-extraction, the 0.1 uF capacitor absorbs the inductive-kick of the opened circuit, minimizing contact-arcing. The -5 VDC side of the supply is artificially loaded, providing a minimum load to improve output voltage regulation. The power-up reset generator, assures that RESET is active while the +5 VDC supply is between 1 and 4.5 VDC. This guarantees proper configuration of the Xilinx FPGA during hot swapping and power-up.

3.3.2 VOLTAGE CONTROLLED OSCILLATOR (Sheet 7)

The card is equipped with a 32.768 MHz VCO. This VCO is phase locked to a 1 MHz reference frequency that is derived from REF A, B, and C inputs (FREQIN). The FPGA provides a divider and phase-comparator for the FREQIN signal and the 32.768 MHz on-board oscillator. The filtered phase comparison output from the loop filter integrator connects to the voltage control input on the 32.768 MHz oscillator; closing the loop. The

32.768 MHz output is the clock source for the six DDS frequency synthesizer ICs.

3.3.3 FPGA / DDS (Sheets 4, 5, & 6)

FPGA U4 provides the timing and control signals for the N8 synthesizer in both LOCAL and CPU modes. When the N8 is operated in LOCAL mode, frequency select switches SW4 and SW3-1 are used to program the six synthesizer ICs with the same output frequency rate. After the FPGA sets the frequency registers in all six DDS ICs, all six DDS ICs are synchronized to the Primary or Secondary synchronization input (if this function is enabled). This synchronization input allows the N8 frequency rates to not only be frequency locked but to also be phase synchronized to the other outputs in the system.

In a system that includes a Fault Monitor/CPU assembly, the FPGA is the interface between the N8 Frequency Synthesizer and the CPU. When the N8 card is operated in the CPU mode, the Fault Monitor/CPU assembly sets the N8's six DDS ICs with the previously stored Output A through F values. The DDS ICs are individually re-synchronized (if the synchronization function is enabled) whenever the CPU writes a new frequency value to that IC.

3.3.4 FILTERS / COMPARATORS (Sheet 6)

The differential sine wave outputs from each DDS IC are connected through an LC filter to a voltage comparator. The voltage comparators convert the differential sine waves to single-ended outputs.

3.3.5 OUTPUT DRIVERS (Sheet 7)

When the N8 card is configured for RS-422 output mode, the card uses two quad RS-422 drivers to output the 6 differential pairs. This mode provides true RS-422 compliant outputs. When the card is operated in TTL mode, three more RS-422 output drivers are connected in parallel with each of the six non-complementary OUTPUT A through F drivers. These drivers provide extra output current for driving 50 ohm loads.

The output signals, whether single-ended or differential, are square waves. In TTL mode, driving 50 ohms to ground, the output levels are basically TTL: 0 VDC and 3 VDC. In RS-422 mode, driving 100 ohms between +Output and -Output, the output levels are RS-422 compatible: 1 VDC and 4 VDC.

3.3.6 FAULT DETECTION (Sheets 4, 7 & 9)

There are three categories of fault detection: Input, Output and PLL faults. All three fault detector categories use a combination of discrete components and Xilinx FPGA logic to perform the detection task.

N8 phase synchronization inputs, Primary and Secondary, are detected for voltage levels using voltage comparators. The synchronization signals are then qualified for activity (if enabled) by the FPGA. Watchdog timers inside the FPGA compare the synchronization signals to the Delay switch time-out setting. If both Primary and Secondary synchronization input sources are deemed bad, the FPGA communicates this condition to the SYNTH FAULT LED and to the CPU card (if installed).

The output driver fault detector consists of two 1 of 8 analog multiplexers that sample 12 outputs in RS-422 mode or 6 outputs in TTL mode. The multiplexers are under control of the FPGA. The multiplexers sample each of the outputs and pass the sampled output to a mono-stable that is used as a watchdog timer. If the sampled output is not switching (bad), the output from the watchdog timer will provide a logic high to the FPGA, which recognizes this as an output signal fault. Logic inside the FPGA continually verifies the condition of each output. Failure to detect a signal from an output results in activation of the appropriate OUT fault indicator and reports the failure to the CPU card (if installed).

The N8 Frequency Synthesizer (SYNTH FAULT) detector utilizes four voltage comparators to detect an out-of-lock condition in the 32.768 MHz VCO. These comparators verify that the VCO control voltage and filtered phase comparator voltage are within defined limits. If the control voltage is out of tolerance, circuitry in the FPGA is activated and communicates this condition to the SYNTH FAULT LED and to the CPU card (if installed).

3.3.7 BACKPLANE FAULT OUTPUT

Inside the FPGA, all faults are combined to form a composite fault signal, which is used to drive the Fault line to the Fault Monitor CPU. Fault-signal active indicates status-bit true. (Note that FAULT signal is active low on the backplane.) Refer to manual section 2.5.4 for detailed information on the fault reporting.

3.3.8 FAULT INDICATORS (Sheet 10)

The INIT. FAULT indicator is driven by the FPGA Initialization-done signal. It activates during initialization, and remains active if initialization does not complete. This is an extremely unusual occurrence.

The SYNTH. FAULT indicator is powered directly from the backplane 48 VDC power buss and is controlled via an opto-isolator to maintain 48 VDC isolation. If local 5 VDC power is lost, the SYNTH. FAULT indicator will be ON solid.

3.3.9.1 SYNCHRONIZATION INPUT FAULT

The SYNTH. FAULT indicator is not turned ON from this fault source if either the Primary or Secondary synchronization inputs are viable or if the synchronization function is disabled. If both the Primary and Secondary inputs are lost and the function is enabled, the SYNTH. FAULT indicator will blink ON and OFF.

3.3.9.2 PLL FAULT

The SYNTH. FAULT indicator is not turned ON from this fault source when the 32.768 MHz VCO is locked and functioning within limits. When the 32.768 MHz VCO is not locked, the SYNTH. FAULT indicator will blink ON and OFF.

3.3.9.3 OUT FAULT

The OUT fault indicators are controlled directly by the fault detection logic. NOTE: In RS-422 mode, OUT A through F LEDs indicate when either a non-complimented or complimented output fault condition exists.

SECTION FOUR

4 DETAILED DRAWINGS

4.1 560-5303 DETAILED DRAWINGS / BILL OF MATERIALS